

No. of Printed Pages : 03

Roll No.

AA-765

M. Tech. EXAMINATION, May 2018

(First Semester)

(B. Scheme) (Re-appear Only)

ECE(VLSI)

MTVLSI509

ADVANCED COMPUTER ARCHITECTURE

Time : 3 Hours]

[Maximum Marks : 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

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P.T.O.

Unit I

1. (a) What is the concept of program partitioning and scheduling ? Explain. 7½
(b) What are Demand Driven Mechanisms ? Explain. 7½
2. (a) Compare Hardware and Software parallelism. Use particular case to explain. 7½
(b) What are Data and resource dependences ? Explain. 7½

Unit II

3. (a) Compare vector and symbolic processors. 7½
(b) Explain the structure and working of CISC processor. 7½
4. (a) Explain the concept of crossbar switch and multiport memory. 7½
(b) Enumerate the properties of network and explain how routing is implemented. 7½

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Unit III

5. (a) Explain computer arithmetic principles. 6
(b) Explain how multifunctional arithmetic pipelines. 6
(c) Explain structure of cache. 3
6. (a) What are memory hierarchies ? How these are designed ? 7½
(b) What is Pipelining ? What are the steps involved in the design of pipeline ? How instruction scheduling is affected by design of pipelining ? 7½

Unit IV

7. (a) What are memory based directory protocols ? Explain. 7½
(b) What are various models of memory consistency ? Explain. 7½
8. Write short notes on the following :
(a) Fault Tolerance system
(b) Cache coherence. 15

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