Unit IV

7. Explain carry look Ahead Adder and design 16-bit cary generator circuits. Also, design 4-bit carry generator circuits by using CMOS Technology. **15**

8. Write short notes on the following : **15**

(a) PLA

(b) Wallace Tree multiplier.

No. of Printed Pages : 04 **Roll No. .....**

AA-763

M. Tech. EXAMINATION, Dec. 2017

(First Semester)

(B. Scheme) (Main & Re-appear)

ECE(VLSI)

MTVLSI-505

DIGITAL CMOS IC DESIGN

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. Each question carries equal marks.

Unit I

1. Mention what are three regions of operation of MOSFET and how are they used ? Find the drain current for an nMOS having $\mu_n C_{ox}$ = 180 μA/V^2, W = 5 μm. L = 0.25 μm, V_{GS} = 1.5 V, V_{tn} = 0.5 V, V_{DS} = 1.0 V. **15**

2. (a) What is CMOS latchup ? How it can be prevented ? **10**

(b) Give the expression for pull-up to pull-down ratio (*Zpu*/*Zpd*) for an nMOS inverter driven by another nMOS inverter. **5**

Unit II

3. What are design rules ? Explain design rules for different layers, PMOS, NMOS and contact cut. **15**

4. (a) Calculate the ON resistance for VDD to GND for the nMOS and CMOS inverter circuits. **7**

(b) Discuss the principle of constant field scaling and also write its effect on device characteristics. **8**

Unit III

5. (a) Design the following function by using static and dynamic CMOS logic : **9**

(i) Three input NAND Gate

(ii) F = AB + C.

(b) What do you mean by two phase clocking and its generator with diagram ? **6**

6. (a) Explain CMOS Schmitt Trigger with its characteristics. **9**

(b) Design negative edge triggered D-FF using transmission gate. **6**