**No. of Printed Pages : 03** **Roll No. .....**

# AA-763

## M. Tech. EXAMINATION, May 2017

(First Semester)

(B. Scheme) (Re-appear Only)

ECE(VLSI)

MTVLSI-505

DIGITAL CMOS IC DESIGN

*Time :* 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

**Note** : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

## Unit I

**1.** (a) Determine pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter. **10**

(b) What is difference between transmission time and propagation delay ? Explain with reference to CMOS logic. **5**

**2.** (a) Explain various techniques to reduce static and dynamic power dissipation. **8**

(b) Briefly explain DC transfer characteristics of BiCMOS inverter. **7**

## Unit II

**3.** (a) Discuss briefly about layout design rules. **7**

(b) What is scaling concept ? Discuss the scaling factors for device parameters. **8**

**4.** (a) Describe in detail the transistor sizing for the performance in combinational networks. **7**

(b) Derive expressions for effective resistance and capacitance estimation using RC delay models. **8**



## Unit III

**5.** Discuss charge-sharing problem in VLSI circuits. Explain various techniques used in domino CMOS circuits for solving this problem. **15**

**6.** (a) Discuss voltage transfer characteristics of pass-transistor AND gate. **7**

(b) Implement D flip-flop using transmission gate. **8**

## Unit IV

**7.** Illustrate the design process of : **15**

(a) Serial-parallel multiplier

(b) Wallace Tree multiplier.

**8.** (a) Discuss about semiconductor memory design issues. **5**

(b) Explain the internal structure of 64KX1 DRAM. Discuss DRAM access with the help of timing diagrams. **10**