(c) How can we optimize a switching activity ? **5**

8. Write short notes on the following :

(a) Design of 4-bit shifter

(b) Low power design. **15**

AA-63

M. Tech. EXAMINATION, Dec. 2017

(First Semester)

(B. Scheme) (Main & Re-appear)

ECE/Industry Integrated

MTEC-505-B

DIGITAL VLSI DESIGN

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Explain the VLSI design flow. **5**

(b) Explain how computer-aided design technology. **5**

(c) What are small device models ? Explain. **5**

2. (a) How we can compute propagation delays in VLSI circuits ? **7**

(b) What is Noise Margin ? How it affects the operation of VLSI circuits ? **5**

(c) Draw the circuit diagram of CMOS inverter. **3**

Unit II

3. (a) What are the rules of drawing stick diagrams ? **5**

(b) Draw and explain inverter layout. **4**

(c) Explain switching characteristics of CMOS. **6**

4. (a) What is Scaling Factor ? Explain, how scaling is done in VLSI circuits ? Explain with the help of specific parameters and components. **8**

(b) How can we estimate resistance of CMOS as a performance parameter ? **7**

Unit III

5. (a) What is clocked CMOS logic ? Explain.

(b) What complimentary switch logic ? Explain. **7½**

(c) Explain the working of CMOS schmitt trigger. **7½**

6. Compare and contrast static, dynamic and differential logic families with the help of specific designs and circuits. **15**

Unit IV

7. (a) Design 4 bit look ahead carry circuit. **5**

(b) Explain the concept of Braun array. **5**