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M. Tech. EXAMINATION, May 2018

(First Semester)

(B. Scheme) (Re-appear Only)

(ECE/INDUSTRY INTEGRATED)

MTEC505B

DIGITAL VLSI DESIGN

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting *one* question from each Unit.

Unit I

1. (a) Explain design hierarchy of VLSI circuits. **5**

(b) Explain the concept of geometric scaling theory. **5**

(c) Write short note on noise margin. **5**

2. (a) How can we compute power consumption of a VLSI circuit ? Also explain how the power consumption be reduced ? **7½**

(b) Explain transfer characteristics of MOS inverter. **7½**

Unit II

3. Draw and explain layout for the following :

(i) CMOS NAND gate

(ii) CMOS Ex-OR gate. **7½,7½**

4. (a) Explain how scaling is done ? What are the different issues involved in it ? **7½**

(b) Explain how capacitance estimation is being done ? **7½**

Unit III

5. (a) What is CMOS domino logic ? Explain. **5**

(b) Explain pass transistor logic. **5**

(c) Explain complementary switch logic. **5**

6. Design the following circuits : **15**

(a) Sample and hold circuit

(b) CMOS Schmitt trigger

(c) Master-slave flip-flop.

Unit IV

7. (a) Draw and explain design of an ALV subsystem. **7½**

(b) Explain design of serial-parallel multiplier. **7½**

8. Write short notes on the following :

(a) Low Power Design **7½**

(b) Optimization of Switching Activity. **7½**