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18AA1201

M. Tech. EXAMINATION, May 2019

(First Semester)

(C Scheme) (Re-appear)

ECE(VLSI)

MTVLSI501C

RTL Simulation and Synthesis with PLDs

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. Explain need and design strategies for multi-clock domain designs. **15**

2. (a) Write an entity declaration for a 4 bit magnitude comparator. Name the output port altb for "a less than b".

(b) Write four architecture bodies for the entity declaration in Question 2(a) (above): One using an if-then-else statement, one using Boolean equations, one using a when-else statement, and one using component instantiation statements.

Unit II

3. (a) What are Programmable logic devices ? Explain in details. **8**

(b) What is ESD protection ? Explain in details. **7**

4. (a) What is floor planning ? Explain with proper illustrations. **8**

(b) What is Power Analysis ? Why is it important for VLSI circuits. **7**

Unit III

5. Enlist and explain low power VLSI design techniques. **15**

6. (a) What are the sources of power dissipation in VLSI circuits ? **8**

(b) Explain dynamic power supression in VLSI systems. **7**

Unit IV

7. Explain I.P. in different forms. **15**

8. Write short notes on the following : **15**

(a) Netlist

(b) Physical IP

(c) Speed issues.