

No. of Printed Pages : 03

Roll No. ....

**AA-762**

**M. Tech. EXAMINATION, May 2018**

(First Semester)

(B. Scheme) (Re-appear Only)

ECE(VLSI)

MTVLSI503

VLSI FOR OPTICAL INTERCONNECTS

*Time : 3 Hours]*

*[Maximum Marks : 75*

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Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

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**Note :** Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

(2-13/13) M-AA-762

**P.T.O.**

### Unit I

1. (a) Discuss properties of Random Binary Data and explain its generation process. **8**  
(b) Explain the effect of low pass filtering on random data and periodic data. **7**
2. (a) Explain design and working of distributed feedback laser. **5**  
(b) Give model for chromatic dispersion. **5**  
(c) Comment on responsibility and efficiency of Avalanche diode. **5**

### Unit II

3. (a) Design a CMOS TIA to handle overload response. **10**  
(b) What are noise sources in feedback TIA configuration ? **5**
4. (a) What are various performance parameters of limiting amplifier ? **5**  
(b) Derive SNR of TIA. **5**  
(c) What is significance of AM/PM conversion ? **5**

**M-AA-762**

**2**

### Unit III

5. (a) Design a ring oscillator using CMOS inverters. **8**  
(b) Discuss design of a VCO to equalize rise and fall time. **7**
6. (a) Design CMOS multiplexer in :  
(i) tree structure topology  
(ii) shift register topology. **10**  
(b) What are various metrics used to quantify modulator driver circuit ? **5**

### Unit IV

7. (a) How is performance of interconnect measured ? **5**  
(b) Differentiate electrical and optical interconnects. **10**
8. (a) Draw :  
(i) Delay vs. technology node (nm) graph  
(ii) Power dissipation vs. Technology Node (nm) graph. **10**  
(b) How is link efficiency measured ? **5**

**(2-13/14) M-AA-762**

**3**

**20**