(d) Determine the pipeline throughput.

(e) Determine the lower and upper bound on the MAL for this pipeline. **3×5=15**

Unit III

5. (a) Compare the relative merits and demerits of the fully associative cache and set associative cache memory organization ? **10**

(b) Explain why a superpipelined processor performs less effectively than a superscalar processor of small degree ? **5**

6. (a) Why do we need hierarchical memory ? Give reasons to support your answer. **5**

(b) Explain the difference between superscallar and VLIW architecture in terms of hardware and software requirements. **10**

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BB-581

M. Tech. EXAMINATION, May 2017

(Second Semester)

(B. Scheme) (Main & Re-appear)

(CSE)

CSE-502-B

ARCHITECTURE OF HIGH PERFORMANCE COMPUTER SYSTEMS

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. Explain, how instruction set, compiler technology, CPU implementation and control, and cache and main memory affect the CPU performance and justify the effects in terms of program length, clock rate and effective CPI. **15**

2. A workstation uses a 15 MHz processor with a claimed 10 MIPS ratting to execute a given program mix. Assume a one-cycle delay for each memeory access.

(a) What is effective CPI of this computer ? **5**

(b) Suppose the processors is being upgraded with a 30 MHz clock. However, the speed of memory subsystem remains unchanged, and consequently two clock cycles are needed per memory access. If 30% of instructions required one memory access and another 5% require two memory accesses per instruction. What is the performance of the upgraded processor with a compatible instruction set and equal instruction counts in a given program mix ? **10**

Unit II

3. Describe different types of hazards and the techniques used for handling hazards ? **15**

4. Consider the following reservation tables for a four stage pipeline with the clock cycle $t = 20$ ns.

	1	2	3	4	5	6	7	8
S_1	X					X		X
S_2		X		X				
S_3			X		X		X	

(a) What are the forbidden latencies, permissible latencies and initial collision vector ?

(b) Draw a state transition diagram for scheduling the pipeline.

(c) Find out greedy cycles and the MAL associated with the shortest greedy cycles.

Unit IV

7. How is memory consistency maintained in shared memory architecture ? Explain in detail with the help of an example. **15**

8. Write short notes on the following :

(a) Data flow computers **8**

(b) Cluster computers. **7**

Unit IV

7. How is memory consistency maintained in shared memory architecture ? Explain in detail with the help of an example. **15**

8. Write short notes on the following :

(a) Data flow computers **8**

(b) Cluster computers. **7**