Unit IV

7. (a) Give the approaches to message passing in computer clusters. **5**

    (b) What are systolic architectures ? **10**

8. Discuss the Von Neumann bottleneck. What are various methods for mitigating Von Neumann bottleneck ? **5+10=15**

18BB1010

M. Tech. EXAMINATION, May 2019

(Second Semester)

(C Scheme) (Main Only)

CSE

MTCSE546C

Architecture of High Performance Computer Systems

Time : 3 *Hours*]   [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Marks are indicated against each question. Attempt any *five* questions selecting at least *one* question from each Unit.

Unit I

1. (a) Differentiate between CISC and RISC architectures and their applications. **5**

(b) Can RISC is better than CISC ? **5**

(c) How is the principle of locality is exploited and what are its different types ? **5**

2. (a) Every instruction in RISC subset can be implemented in at most five clock cycles. Name these clock cycles. **5**

(b) Suppose that we want to enhance the processor used for web serving. The new processor is 10 times faster in computation in the web serving application than the original processor. Assuming that the original processor is busy with computation 40% of the time and is waiting for I/O 60% of the time. What is overall speedup gained by incorporating the enhancement ? **10**

Unit II

3. (a) What is branch prediction buffer ? **5**

(b) What are tournament predictors and their relative merits and demerits ? **10**

4. (a) How compiler can increase the amount of available ILP by transforming loops ? Give an example. **10**

(b) What is correlating predictor ? **5**

Unit III

5. (a) What are the limitations of superscalar processing ? **7**

(b) How loop interchange, merging arrays and blocking can reduce cache misses ? **8**

6. (a) Give the working principle of VLIW processor. **7**

(b) How we can use the coherence mechanisms of a multiprocessor to implement spin locks ? **8**