(b) Explain Design of PLL using CMOS. **7½**

**8.** Write short notes on the following :

(a) OTA Amplifier **7½**

(b) Switched Capacitor. **7½**





# BB-64

## M. Tech. EXAMINATION, May 2018

(Second Semester)

(B. Scheme) (Main & Re-appear)

(ECE/Industry Integrated)

MTEC508B

ANALOG VLSI DESIGN

*Time :* 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

**Note** : Attempt any *Five* questions out of given eight at least *one* question from each Unit. All questions carry equal marks.

## Unit I

**1.** (a) Compare the phenomenon of strong and weak inversion. **5**

(b) Draw the small signal model of MOS. Also explain the each component in the small signal model account for. **7**

(c) What do you mean by level-3 model ? **3**

**2.** (a) Explain, how MOS switch works ? **4**

(b) CMOS Regulated cascade current source is used for what purpose ? Draw its circuit and explain the working. **7**

(c) Explain working of MOS Switch. **4**

## Unit II

**3.** Write short notes on the following : **15**

(a) Simple current mirror.

(b) Widlar current mirror.



**4.** Explain the following : **15**

(a) Gilbert Cell

(b) Cascade Amplifier

(c) Resistive Load.

## Unit III

**5.** (a) Design a two stage MOS amplifier using OP-Amp. **7½**

(b) What is Op-amp stability and frequency compensation ? Explain. **7½**

**6.** (a) Design a two-stage CMOS Comparator. **7½**

(b) What are the various parameters involved in the design of a comparator using CMOS ? Explain in brief. **7½**

## Unit IV

**7.** (a) Design a VCO using CMOS and Op-Amp. **7½**