No. of Printed Pages : 03 **Roll No. .....**

BB-765

M. Tech. EXAMINATION, Dec. 2017

(Second Semester)

(B. Scheme) (Re-appear Only)

ECE(VLSI)

MTVLSI-560

IC FABRICATION TECHNOLOGY

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Explain CZ technique of wafer preparation. Calculate max pull rate for 6" wafer. **10**

(b) What are various epitaxial defects. **5**

2. (a) Compare epitaxy techniques. **5**

(b) Discuss growth kinetics of VPE. **10**

Unit II

3. (a) Compare wet and dry oxidation. **8**

(b) Graphically show masking property of SiO_2. **7**

4. (a) How does oxidation rate change with thickness of oxide ? **7**

(b) Discuss growth physics for diffusion from doped oxide source. **8**

Unit III

5. (a) Outline basic physics behind lithography. **8**

(b) What are major drawbacks of wet etching ? How is it removed ? **7**

6. (a) Differentiate physical and chemical etching. **7**

(b) Explain commonly used dry etching system. **8**

Unit IV

7. Write short notes on the following : **15**

(i) FDSOI

(ii) 3-D CMOS

(iii) Coulomb Blockade.

8. (a) What are integration issues involved with ultra thin body SOI ? **8**

(b) How is FinFET different from MOSFET ? **7**