

8. (a) What are the applications of layout compaction ? 7½
- (b) Explain the Constraint-Graph Based Hierarchical Compaction. 7½

No. of Printed Pages : 04

Roll No.

CC-65

M. Tech. EXAMINATION, May 2017

(Third Semester)

(Re-appear Only)

ECE(Industry Integrated)

MTEC-609-B

ALGORITHM FOR VLSI DESIGN

Time : 3 Hours]

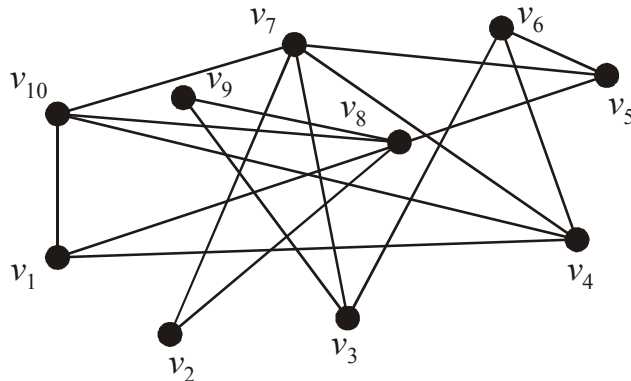
[Maximum Marks : 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks. Use of calculator is allowed.

Unit I

1. (a) Discuss different design styles involved in VLSI physical design. 7½
(b) Distinguish between Depth-First search and Breadth-First search methods. 7½
2. Partition the graph shown in Figure below, using Kernighan-Lin algorithm. 15



Unit II

3. (a) Discuss the Classification of Pin Assignment Algorithms. 7½
(b) Explain Integer programming based floor planning. 7½

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4. (a) Explain problems associated during placement in physical design process. 7½
(b) Discuss the Force Directed Placement algorithm. 7½

Unit III

5. (a) Discuss the different phases in global routing. 7½
(b) Explain Lee's and Soukup's Maze Routing algorithms. 7½
6. (a) What are the parameters associated with the routing problems and explain ? 7½
(b) Explain single layer routing algorithms. 7½

Unit IV

7. (a) Compare different Two-Layer Over-the-Cell routing algorithms. 7½
(b) Explain Unconstrained Via Minimization. 7½

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