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CC-766

M. Tech. EXAMINATION, May 2018

(Third Semester)

(Re-appear Only)

ECE(VLSI)

MTVLSI661

CMOS RF IC DESIGN

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. Briefly describe the following wrt RF Design : **8+7**

(a) Power efficiency, Noise and Dynamic range

(b) Random process, Non-linearity and Time variance.

2. (a) Compare Coherent and Non-coherent detection techniques. **7**

(b) What do you understand by the term Inter-symbol interference and conversion of gains in RF circuits ? Discuss in detail the working of Digital modulation. Also, give its various advantages, disadvantages and applications. **8**

Unit II

3. Discuss the following in detail : **7+8**

(a) Direct conversion transmitter

(b) Digital-IF receiver and Spice model.

4. Define the terms Homodyne receiver and Image-reject receiver. Also, explain the concept of BJT behaviour at RF frequencies. **15**

Unit III

5. Define the terms VCO, Noise power and Mixer. Also, discuss in detail the Low noise amplifier design in RF circuits. **15**

6. Describe the working of the following : **8+7**

(a) CMOS LC Oscillator

(b) Quadrature signal and signale generators.

Unit IV

7. Explain the operation of the following in detail : **8+7**

(a) RF Synthesizer

(b) PLL.

8. Write short notes on the following : **8+7**

(a) High frequency power amplifier

(b) Liberalization techniques.