(b) Describe the major DRAM feature and parameter that affect a high performance memory system design. **7.5×2=15**

6. (a) On which parameters the minimum storage capacitance of a DRAM cell depends ? Discuss the various approaches by which cell storage charge can be increased.

(b) Explain Read-Modify. Write operation of DRAM. **7.5×2=15**

Unit IV

7. (a) Explain the Fowler-Nordheim tunneling mechanism used in EPROM cells.

(b) Draw and explain functional block diagram of NAND flash memory cell. **7.5×2=15**

8. (a) Compare NOR, NAND and DINOR based architecture flash memories.

(b) What is mutlilevel technique in Non-Volatile Memories ? Explain the factors on which multiplicity of charge storage technique depends. **7.5×2=15**

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CC-770

M. Tech. EXAMINATION, May 2017

(Third Semester)

(Re-appear Only)

ECE(VLSI)

MTVLSI-663

DESIGN OF SEMICONDUCTORS MEMORY

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks. Use of calculator is allowed.

Unit I

1. Consider a standard 6-T SRAM cell.

Use the following parameters.

L = 300 nm, VDD = 2.5 V.

For all the NMOS transistors, allowed minimum and maximum widths are 450 nm and 1800 nm, respectively. Always size the pull-up PMOS transistors as three-times the widths of the pull down NMOS transistors. You should consider widths in 50 nm intervals.

Write your assumptions with clear and concise explanation for all the parts below.

Determine :

(i) Cell ratio (ratio of the widths of pull-down NMOS and access transistor) for read operation

(ii) Pull-up ratio (ratio of the widths of pull-up PMOS and access transistor) for write operation.

V_{tn0} = 0.431 V, V_{tp0} = –0.616 V.

Also $\mu_{n0} = 455.4\ cm^2/V/S$, $\mu_{p0} = 158.7\ cm^2/V/S$

2. What is the significance of Static Noise Margin. Explain Read SNM and write SNM. List the various techniques to measure Read SNM and write SNM. **15**

Unit II

3. (a) Draw and explain the Divided Word Line (DWL) and Hierarchical Word Decoding (DWD) decoder structures.

(b) Why is Sense Amplifier Circuit required in SRAM cell ? Explain the working of current mirror differential sense amplifier circuit. **7.5×2=15**

4. (a) Compare the performance of CAM with SRAM cell.

(b) Explain the different sources of power dissipation in SRAM cell.

Unit III

5. (a) Explain memory read and memory write operation sequences of SDRAM.