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18C3

B. Tech. EXAMINATION, 2020

(Third Semester)

(C Scheme) (Main & Re-appear)

(CSE)

ECE203C

DIGITAL SYSTEM DESIGN

Time : 2½ *Hour*s] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Four* questions in all. All questions carry equal marks.

1. (a) Simplify the following expression using Boolean algebra :

$$F = A + B\left[AC + \left(B + \overline{C}\right)D \right]$$

(b) Realize XOR function using NOR logic.

(c) Simplify the following expression using K-map and implement it using NAND Gates only :

$F = \Sigma m(0, 1, 4, 5, 6, 13, 14, 15, 22, 24, 25, 28, 29, 30, 31)$

2. (a) Reduce the following expression using 3-variable Map :

$$F = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}CD + \overline{A}B\overline{C}\,\overline{E} + \overline{A}B\overline{C}E + A\overline{B}C + ABC + AB\overline{C}\,\overline{D}$$

(b) Design and implement a BCD to Excess-3 code converter using suitable logic gates.

3. (a) Implement the following function using 8 : 1 MUX :

$$F = \Sigma m(0, 1, 3, 4, 5, 8, 9, 15)$$

(b) Design a full substractor using 3 : 8 decoder.

(c) Implement a 16 : 1 MUX using 4 : 1 MUX ICs.

4. (a) Design and implement a Mod-6 synchronous counter using J-K flip-flop.

(b) What is meant by universal shift register ? Explain the working of a 4-bit universal shift register with the help of its functional table.

5. (a) Design a serial binary adder using D flip-flop.

(b) Design a sequence detector to detect the non-overlapping sequences 1011 and 1101. It generates output 1 when sequence is detected.

6. (a) Discuss the components and features of ASM chart.

(b) Draw an ASM chart and state table for a 2-bit up/down counter having mode control input M such that M = 1 for up counting and M = 0 for down counting. The circuit should generate output 1 whenever the count becomes minimum or maximum.

7. (a) Explain working of a two-input TTL NAND gate with the help of circuit diagram.

(b) How is propagation delay improved in totem-pole TTL logic ?

(c) What is current sinking logic ?

8. (a) What are the advantages of PLDs over fixed function ICs ?

(b) Compare CPLD and FPGA.

(c) Design and implement 4-bit Binary to Gray code converter using PLA.