

7. A certain vector processor has a cycle time of 8 ns and memory cycle of 64 ns. It uses 8 modules and does not bypass requests in the memory buffer. For a sustained vector environment of two requests per cycle :

- (a) What is requested (offered) memory bandwidth in Mbps ?
- (b) What is achieved memory bandwidth in Mbps ?
- (c) What is mean queue size of requests waiting for memory ?

8. (a) What do you mean by orthogonal instruction set ? Why is it so important in modern machines ? **10**

- (b) Explain virtual address to real address translation process with suitable diagram. **10**

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B. Tech. EXAMINATION, May 2017

(Seventh Semester)

(Old Scheme) (Re-appear Only)

(CSE)

CSE-405(NEW)/CSE-401(OLD)

ADVANCED COMPUTER ARCHITECTURE

Time : 3 Hours]

[Maximum Marks : 100

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt any *Five* questions. Each question carries equal marks.

1. Explain with the help of diagrams the following cache coherency protocols : **20**
 - (a) Write Invalidate Protocol
 - (b) Berkeley
 - (c) Illinois.
2. (a) What are the different methods to detect the parallelism in a program ? Briefly discuss each. **10**
 - (b) How different addressing modes are helpful for computer programmers ? Explain any *three* types of addressing modes. **10**
3. What are different types of clocking used during data transfer among registers ? Discuss various types of clocking overheads for single rank registers. **20**
4. What are different types of dependencies encountered during out-of-order execution and multiple instruction execution ? How these dependencies are handled ? **20**

5. Suppose two processors (in a multiple processor system) make a total of exactly two references to memory every memory cycle ($T_c = 100$ ns). The memory consists of eight low-order interleaved memory modules with $T_{\text{access}} = 120$ ns. Find : **20**
 - (a) Expected Waiting Time (T_w)
 - (b) Total access time
 - (c) Mean total number of queued (waiting) requests
 - (d) Offered memory bandwidth (references/sec)
 - (e) Achieved memory bandwidth (references/sec).
6. (a) How the concept of colored pages is used in physically addressed caches ? Explain its pro and cons. **10**
 - (b) What is associative memory ? Derive match logic for one word of associative memory ? **10**