Unit III

5. (a) Describe in detail the DSB model for weak memory consistency. **10**

(b) Give Lamport's definition of sequential consistency. **5**

6. Explain the following terms associated with memory management : **15**

(a) Role of memory manager if OS kernel.

(b) Preemptive *Vs* Non-preemptive memory allocation policies.

(c) Demand Pageing memory system and example.

Unit IV

7. Vectorize or parallelize the following loops if possible. Otherwise explain why if it is not possible to do so : **15**

(a) Do I = 1, N
A(I + 1) = A(I) + 3.14159
Enddo.

G-15

B. Tech. EXAMINATION, May 2017

(Seventh Semester)

(Electives) (Re-appear Only)

(CSE)

CSE-455-B

ADVANCED COMPUTER ARCHITECTURE

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. Explain, how instruction set, compiler technology, CPU implementation and control and cache memory hierarchy affects the CPU performance and justify the affects in terms of program length, clock rate and effective CPI. **15**

2. (a) Explain the applicability and restrictions involved in using the Amdahl's law, Gustafson's law to estimate the speedup performance of an *n*-processor system compared to that of a single processor system. Ignore all communication overheads. **10**

(b) List five applications of parallel processors. **5**

Unit II

3. (a) Draw and explain the instruction format of atypical VLIW based machine. **7**

(b) Compare the features of RISC and CISC architectures. **8**

4. Consider the five stage pipelined processor specified by following reservation table : **15**

	1	2	3	4	5	6
S1	×					×
S2		×			×	
S3			×			
S4				×		
S5		×				×

(a) List the set of forbidden latencies and collision vector.

(b) Draw state transition diagram showing all possible initial sequences (cycles) without causing a collision in pipeline.

(c) List all simple cycles from state diagram.

(d) Identify greedy cycles among the simple cycles.

(e) Calculate the minimum average latency (MAL) of pipeline.

(b) Do I = 1, N
if (A(I) .LE. 0.0) then
S = S + B(I) * C(I)
X = B(I)
Endif
Enddo.

8. (a) Explain, how the performance of a parallel computer can be enhanced by Visualization and performance tuning support. **8**

(b) List the different types of concurrencies that can be found in object oriented programming models. Briefly explain the COOP model of computing. **7**

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