Unit IV

7. A sequential circuit has two pulses x inputs x_1 and x_2. The output of circuit becomes 1 when one or more consecutive x_1 pulses are followed by two x_2 pulses. The output then remains 1 for all subsequent x_2 pulses until an x_1 pulse occurs :

(a) Derive minimal state table describing circuit operation.

(b) Synthesize circuit using S-R flip-flip. **15**

8. (a) Write procedure steps required for synthesis of SIC fundamental mode circuits. **8**

(b) Write note on reduction of output dependency. **7**

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B.Tech. EXAMINATION, May 2019

(Fourth Semester)

(B. Scheme) (Main & Re-appear)

(ECE)

ECE204B

DIGITAL CIRCUIT AND SYSTEM

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Explain partition and lattices in detail. **9**

(b) What do you understand by ordered pair and relations ? **6**

2. (a) Using K-map simplify the following function :

$f(a, b, c, d, e) = \Sigma m(1, 2, 4, 5, 9, 11, 13, 14, 16, 18, 22, 23, 26, 29, 30, 31)$. **7½**

(b) Using Boolean Algebra minimize the following function :

$$y = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD + ABC\bar{D} + A\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D$$

7½

Unit II

3. (a) Explain analysis and synthesis of NAND-NOR circuits. **7**

(b) Design a BCD-to-decimal Decoder. **8**

4. (a) Explain the steps of synthesis of threshold networks. **7**

(b) The function $f(w, x, y, z) = \Sigma 1, 3, 10, 6$ 13, 15 can be decomposed to form $F[\phi(v, y, z)\ w, x]$. Determine the function F and ϕ. **8**

Unit III

5. A clocked sequential circuit with single input x and single output z produced an output $z = 1$ whenever input x completes sequence 1011. Also overlapping is allowed.

(a) Obtain state diagram.

(b) Obtain its minimum state table and design circuit with T-flip-flop. **15**

6. (a) Explain capabilities and limitations of finite state machines. **8**

(b) Give detailed note on machine equivalence. **7**