## 422

## B. Tech. EXAMINATION, 2020

(Fifth Semester)
(Old Scheme) (Re-appear Only)
(ECE)
ECE204
DIGITAL ELECTRONICS

Time : $2 ½$ Hours]
[Maximum Marks : 100
$\overline{\text { Before answering the question-paper candidates should ensure that they have been supplied }}$ to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt Four questions in all. All questions carry equal marks.

1. (a) Represent the decimal number 346 into :
(i) Binary
(ii) BCD code
(iii) Excess-3 code
(iv) Octal-code.
(b) Perform the following operations :
(i) $10111 \div 100$
(ii) Add (+19) to (-24).
2. (a) Simplify $f=\overline{\mathrm{C}}(\overline{\mathrm{A}} \overline{\mathrm{B}} \overline{\mathrm{D}}+\mathrm{D})+\mathrm{A} \overline{\mathrm{B}} \mathrm{C}+\overline{\mathrm{D}}$ using $k$-map and realized the minimized expression.
(b) Minimize $\overline{\mathrm{A}} \overline{\mathrm{B}} \overline{\mathrm{C}} \overline{\mathrm{D}}+\mathrm{A} \overline{\mathrm{B}} \overline{\mathrm{C}} \mathrm{D}+\overline{\mathrm{A}} \overline{\mathrm{B}} \mathrm{CD}+\mathrm{ABC} \overline{\mathrm{D}}+\mathrm{A} \overline{\mathrm{B}} \mathrm{C} \overline{\mathrm{D}}+\overline{\mathrm{A}} \overline{\mathrm{B}} \overline{\mathrm{C}} \mathrm{D}$ using Boolean algebra.
P.T.O.
3. (a) What is full adder ? Design a circuit for full adder using half adder.
(b) Realize a $1: 16$ DE-MUX from four $1: 4$ demultiplexer.
4. (a) Design a MOD-8 UP counter using T-flip-flop.
(b) Explain the operation of bidirectional shift register.
5. (a) Discuss CMOS NAND and NOR gate.
(b) Explain the switching characteristics of $p$ - $n$ junction diode.
6. (a) What are the performance characteristics of ADC ? Discuss each in brief.
(b) What is the advantage of R-2R ladder network DAC over binary weighted resister DAC.
7. (a) Compare RAM, ROM and EPROM using their structure and storage.
(b) Draw a neat diagram of a PLA and explain the function of each component.
8. Write short notes on any two of the following :
(a) Error detection and correction codes
(b) CPLDs
(c) Sample and hold circuit.
