Sum := *a* XOR *b* XOR carry; carry := (*a* AND *b*) OR (*a* AND carry) OR (*b* AND carry) Result := sum & result (7 down to 1); END IF.

6. (a) Differentiate between FUNCTION and PROCEDURE and explain how are they called.

(b) Write function that converts 5 bit bit-vector to an integer. Write a procedure to compare two bit-vectors representing two's complement signed integers. **5,10**

Unit IV

7. Design the circuit of dedicated path using shift reg, counters and gates for the algorithm given below. Write VHDL code for the circuit so designed. Use the devices of circuit as components in the code :

INPUT n // $n_7n_6.....n_1n_0$

countbit = 0 // for counting number of 0's and 1's

No. of Printed Pages : 05 **Roll No. .....**

F24

B. Tech. EXAMINATION, May 2019

(Sixth Semester)

(B. Scheme) (Main & Re-appear)

(ECE)

ECE306B

HDL BASED SYSTEM DESIGN

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit.

Unit I

1. (a) What are the advantages of using VHDL in digital design ? Draw a flowchart to describe the FPGA based design flow.

(b) Draw and compare typical SRAM cell and Anti-Fuse Cell. **8,7**

2. (a) Explain basic HDL design flow.

(b) Mention Std-Logic libraries available in IEEE library.

(c) Explain Std-Logic type definition

(d) Draw detailed block diagram of Xilinx CLB.

(e) Compare and contrast SRAM and ANTIFUSE FPGAs. **3×5**

Unit II

3. (a) Briefly explain behavioral, dataflow and structural architecture bodies giving examples.

(b) Write a VHDL code to verify the violation of setup-time and hold-time of a D flip-flop. **7,8**

4. Explain transport and inertial delays. Consider a waveform X within the interval 0 to 50 ns. X is low during 0-10 ns, 20-30 ns and 33-35 ns intervals and high during other intervals.

Plot the waveforms for the following VHDL statements :

Z1 <= transport X after 10 ns; Z2 <= X after 10 ns; Z3 <= reject 4 ns X after 10 ns; **15**

Unit III

5. The partial code of a serial-adder is given below. On the basis of this code decide the hardware components required to design serial-adder. Declare a package which contains VHDL code for each H/W component. Write structural description of serial-adder making use of the package.

IF count < 8 then count := count + 1;

counteight = 8 // for looping 8 times

WHILE (counteight ≠ 8)

If (n_0 = 1) THEN countbit = countbit + 1 ELSE countbit = countbit – 1, END IF

n = n >> 1 // shift n right one bit

counteight = counteight + 1;

IF (countbit = 0) THEN OUTPUT 1, ELSE OUTPUT 0, END IF, ASSERT Done. **15**

8. The controller is required that will make the six peripheral segments in a 7-segment LED light move around in a clockwise or counterclockwise direction, depending on the input of the switch W.

(a) Draw state diagram of the controller.

(b) Show next-state table and output table of the controller and derive excitation and output equations.

(c) Write VHDL code for the controller circuit. **15**

counteight = 8 // for looping 8 times

WHILE (counteight ≠ 8)

If (n_0 = 1) THEN countbit = countbit + 1 ELSE countbit = countbit – 1, END IF

n = n >> 1 // shift n right one bit

counteight = counteight + 1;

IF (countbit = 0) THEN OUTPUT 1, ELSE OUTPUT 0, END IF, ASSERT Done. **15**

8. The controller is required that will make the six peripheral segments in a 7-segment LED light move around in a clockwise or counterclockwise direction, depending on the input of the switch W.

(a) Draw state diagram of the controller.

(b) Show next-state table and output table of the controller and derive excitation and output equations.

(c) Write VHDL code for the controller circuit. **15**