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F24

B. Tech. EXAMINATION, 2020

(Sixth Semester)

(B Scheme)

(Re-appear Only)

ECE

ECE306B

HDL Based System Design

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) What are hardware description languages ? By using an example, explain the concept of simulation and synthesis. **8**

(b) Enlist various desing issues of digital system. Briefly discuss computer-aided design tools for designing of digital systems. **7**

2. Differentiate between the following : **8+7**

(a) PLA, PAL and ROM

(b) CPLDs and FPGA

Unit II

3. (a) Define the term VHDL. Using an example, explain the concept of classes and data types, entity and architecture declaration. **9**

(b) Discuss the concepts of overloading, logical operators and types of delays in VHDL. **6**

4. Describe the following by using suitable examples :

(a) Sequential statements, Concurrent statements and Case statements. **8**

(b) Array and Loops. **7**

Unit III

5. Briefly explain the Packages and Libraries in VHDL. Also by using an example discuss application of functions and procedures. **15**

6. What are combinational circuits ? Explain VHDL models and simulation of multiplexers and comparators. **15**

Unit IV

7. Discuss VHDL models and simulation of FSM and Shift registers. **15**

8. Write short notes on the following :

(a) Design of ALU and Memory unit **9**

(b) Design implementation using FPGAs **6**