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W-621

B. Tech. EXAMINATION, Dec. 2017

(Sixth Semester)

(Weekend) (Re-appear Only)

(ECE)

ECE-W-302

MOS IC'S AND TECHNOLOGY

Time : 3 *Hours*] [*Maximum Marks :* 100

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt any *Five* questions. All questions carry equal marks.

1. Explain N-MOS and CMOS fabrication process with neat diagrams. **20**

2. (a) Give derivation for transcnductance Gm for MOS transistor. **7**

(b) Find the drain current for an nMOS having :

$\mu_n C_{ox}$ = 150 μA/V2,

W = 1 μm

L = 0.25 μm

V_{GS} = 1.5 V

V_{tn} = 0.5 V

V_{DS} = 2.0 V

(c) Derive the CMOS Inverter DC characteristics, show all operating regions and explain it.

3. (a) What is photolithography ? Explain its various steps in detail. **10**

(b) Explain the epitaxial growth process in IC fabrication. How it is done ? Why is it neede ? **10**

4. Explain the following :

(a) Resistance Estimation

(b) Capacitance Estimation. **10**

5. Design the following function by using nMOS and CMOS logic. Explain why, NAND gate are preferred over NOR gate ? **20**

6. What do you mean by power dissipation in MOS ICs ? Out of NMOS and PMOS which one is having more power dissipation and why ? **20**

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8. Explain a two-phase non-overlapping clock generator with buffered output on both phases with the help of suitable diagram. **20**