D-113

B. Tech. EXAMINATION, May 2018

(Fourth Semester)

(Old Scheme) (Re-appear Only)

(IT)

IT204

COMPUTER ORGANIZATION AND
ARCHITECTURE

Time : 3 *Hours*]   [*Maximum Marks :* 100

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit.

Unit I

1. (a) Explain Flynn's Classification of Computers. **10**

   (b) Differentiate between the following :
   (i) RISC and CISC
   (ii) Fixed length and variable length instruction formats. **5+5**

2. (a) Explain the concept of stored program control unit. **10**

   (b) Explain the following addressing modes with example : **5+5**
   (i) Indexed Addressing Mode
   (ii) Register Addressing Mode.

Unit II

3. What are different CPU architecture types ? Explain any *two*. **20**

4. (a) What is micro instruction sequencing ? Explain. **10**

   (b) Differentiate between hardwired control unit design method and micro programmed control unit design method. **10**

Unit III

5. (a) What is memory hierarchy ? Explain its importance. **8**

   (b) Explain set associative cache organization scheme. **12**

6. (a) Explain the concept of DMA. **10**

   (b) What do you mean by interrupt ? List various types of interrupts along with their importance and functions. **10**

Unit IV

7. (a) State and explain Amdhal's law. **10**

   (b) What do you mean by pipelining ? Explain. **10**

8. (a) Write goals of Parallelism. **10**

   (b) Write short note on the multiprocessor system. **10**