

8. Write short notes on any *two* of the following :

- (a) Parallel Multiplier
- (b) 4-bit shifter
- (c) PLA.

15

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M. Tech. EXAMINATION, May 2018

(First Semester)

(B. Scheme) (Re-appear Only)

ECE(VLSI)

MTVLSI505

DIGITAL CMOS IC DESIGN

Time : 3 Hours]

[Maximum Marks : 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Derive the CMOS Inverter DC characteristics, show all operating regions and explain it. **11**
(b) What are the advantages of CMOS inverter over the other inverter configurations ? **4**
2. (a) Calculate Propagation delay T_{PHL} for CMOS inverter. **7**
(b) Find the drain current for an nMOS having : **8**
 $\mu_n C_{ox} = 150 \mu A/V^2$,
 $W = 1 \mu m$
 $L = 0.25 \mu m$
 $V_{GS} = 1.5 V$
 $V_{tn} = 0.5 V$
 $V_{DS} = 2.0 V$

Unit II

3. (a) What do you mean by layout why is it essentials in VLSI design ? **6**

- (b) What do you mean by Stick diagram ?
Draw the stick diagram for two inputs NAND Gate. **9**

4. What are different MOSFET Capacitances ?
Discuss each of them with their origins. **15**

Unit III

5. Design the following function by using both transmission gate and CMOS logic : **15**
(a) Three input NOR Gate
(b) $F = (AB + C)D$
6. (a) Why CMOS Nand gate preferred than CMOS Nor gate for implementing combination logic circuits. **6**
(b) Explain high performance dynamic CMOS circuit with suitable diagram. **9**

Unit IV

7. Explain ALU and design 4-bit adder, shift register and multiplier by using MOSFET. **15**