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18BB1010

M. Tech. EXAMINATION, 2020

(Second Semester)

(C Scheme) (Re-appear)

(CSE)

MTCSE546C

ARCHITECTURE OF HIGH PERFORMANCE COMPUTER SYSTEMS

Time : 2½ *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Four* questions in all. All questions carry equal marks.

1. State and prove Amdahl's law for parallel computers.

2. What are different issues involved in the design of a new computer's instruction set ? Explain the instruction set architecture.

3. Differentiate between giving suitable example of each :

(a) Instruction and processor pipeline

(b) Unifunction and multifunction pipeline

(c) Scalar and vector pipeline.

4. Defien the terms fault, interrupt and exception in context of pipeline. List at least *ten* different anomalies or situations covered under one of these terms and give strategy to handle at least *three* of them.

5. (a) With suitable diagram explain the virtual to physical address translation.

(b) Write and explain cache mapping schemes with suitable diagrams.

6. Draw and explain the architecture of a VLIW systems. Describe, how pipeline operations are implemented in VLIW systems. List the five advantages offered by VLIW systems.

7. Describe the following terms associated with multiprocessor system :

(a) Bus-arbitration algorithm

(b) Delta Networks

(c) Multicache coherence problem.

8. Write five features of non-hierarchical loosely coupled multiprocessor system. Draw and explain the Cm^* Architecture.

9. Write short notes on the following :

(a) Cache coherency

(b) Loop optimization

(c) Array processor

(d) Data dependence

(e) Profile driven optimization in compilers.