6. (a) What are various design constraints of a CMOS compartor ? **5**

(b) What are various methods of compensating 2 stage Op-Amp. **10**

Unit IV

7. (a) Implement a simple PLL in CMOS technology. **5**

(b) Write short notes on the following : **10**

(i) PLL as frequency multiplier

(ii) OTA.

8. What are various types of CMOS ADC ? Model a generalized ADC in CMOS technology. **15**

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M. Tech. EXAMINATION, Dec. 2017

(Second Semester)

(B. Scheme) (Re-appear Only)

ECE/Industry Integrated

MTEC-508-B

ANALOG VLSI DESIGN

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Explain graphically, the variation of Gate-Source and Gate-Drain capacitance with Gate-Source Voltage. **7**

(b) Discuss SPICE level-3 Model for CMOS. **8**

2. (a) Model MOSFET as Diode. **9**

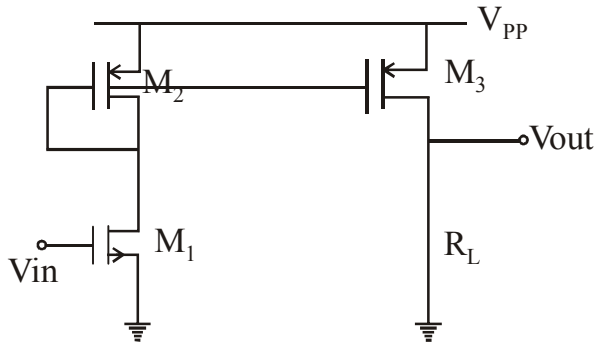
(b) Draw MOS schematic of cascode current sink. **6**

Unit II

3. (a) Derive transconductance of source follower. **7**

(b) What are advantages of differential amplifier ? Draw its small signal equivalent. **8**

4. (a) Calculate small signal voltage gain of the following circuit : **5**



(b) What are application areas of Wilson current mirror ? Draw and explain its small signal equivalent. **10**

Unit III

5. (a) Design a cascode Op-Amp for maximum differential swing of 2.4 V, total power dissipation of 6 mW. **10**

(b) Explain concept of Gain Boosting in Op-Amp. **5**