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BB-765

M. Tech. EXAMINATION, Dec. 2018

(Second Semester)

(B. Scheme) (Re-appear Only)

ECE(VLSI)

MTVLSI560

IC FABRICATION TECHNOLOGY

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit.

Unit I

1. (a) How does surface contamination effect single crystal silicon growth ? **5**

(b) Discuss safety considerations in epitaxial process. **5**

(c) Explain various epitaxial defects. **5**

2. (a) Discuss reaction kinetics of Vapour Phase Epitaxy. **7**

(b) Differentiate Vapour Phase Epitaxy and Molecular Beam Epitaxy. **8**

Unit II

3. (a) Compare techniques and consideration of dry and wet oxidation. **10**

(b) Discuss various masking properties of SiO_2. **5**

4. Give mathematical model of diffusion from a chemical source and doped oxide source. **15**

Unit III

5. (a) Name various optical and electron resists. **5**

(b) Differentiate isotropic and anisotropic etching. **5**

(c) Discuss Trench etching. **5**

6. (a) Discuss various types of and expectations from metallisation. **5**

(b) What are properties of plasma and how these are used for etching ? **10**

Unit IV

7. (a) Explain Ballistic transport in MOSFET. **7**

(b) What are various design considerations in ultra small metallic tunnel functions ? **8**

8. (a) Discuss design issues in ultrathin body SOI. **8**

(b) Explain fabrication steps of vertical transistors. **7**