6. Explain low pass filter and pipelined active RC integrators. **15**

Unit IV

7. (a) Explain the principle of averaging to improve SNR, in mixed signal circuits. **8**

(b) Define SNR, effective number of bits and clock jitter in mixed signal circuit. **7**

8. Write short notes on any *two* of the following :

(a) Guard Ring

(b) Quantization noise

(c) Power supply and ground issue. **15**

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CC-761

M. Tech. EXAMINATION, Dec. 2017

(Third Semester)

(Main & Re-appear)

ECE(VLSI)

MTVLSI-601

MIXED SIGNAL IC DESIGN

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Briefly explain CMOS analog multiplier with the help of a circuit diagram. **8**

(b) Discuss charge pump PLL with neat diagram. **7**

2. Explain how MOSFET behaves as a capacitor. Also explain floating MOS capacitor. **15**

Unit II

3. (a) Describe the simple resistor string DAC, problem associated with it and how is it overcome by use of a binary switch array ? **7**

(b) Find the maximum DNL and INL in LSBs of a 3 bit DAC which has the following characteristics. Check if it is monotonic : **8**

Digital Input	Analog Output
000	0V
001	0.625V
010	1.5625V
011	2V
100	2.5V
101	3.125V
110	3.4375V
111	4.375V

4. Explain various sample and hold architectures and compare it. **15**

Unit III

5. (a) State and explain specification of ADC. **9**

(b) Design a 3-bitflash ADC with its quantization error centred about zero LSB's. Determine the worst case DNL and INL if resistor matching is known to be 5%. Assume that V_{ref} = 5V. **6**